

Sub
A1

- [illegible]

entries representing data more recent than that stored in the data cache memory array, such that a subsequent write operation may free a memory port for a write stored in the bypass structure to be written to the data cache memory array.

4. The system of claim 3 wherein the memory operations are limited to 32 bits, and there are six distinct entries in the bypass system.

5. A method for eliminating stalls in read and write operations to a data cache, comprising steps of:

(a) implementing a bypass system having multiple entries and switching and address matching logic, connected to the data cache memory array by two ports and to a bus for accepting read and write operations;

(b) storing write operations that hit in the cache as entries in the bypass structure before associated data is written to the cache;

(c) searching the bypass structure entries by read operations, using the address matching and switching logic to determine if entries in the bypass structure represent newer data than that available in the data cache memory array; and

(d) using the opportunity of a subsequent write operation to free a memory port for simultaneously writing from the bypass structure to the memory array.

6. The method of claim 5 wherein the memory operations are limited to 32 bits, and there are six distinct entries in the bypass system.